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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Pai-Hung Pan

Serial No.: 09/944,506

Filed: August 30, 2001

For: SHALLOW TRENCH ISOLATION STRUCTURE WITHOUT CORNER EXPOSURE (as amended)

Confirmation No.: 4348

Examiner: G. Fourson III

Group Art Unit: 2823

Attorney Docket No.: 2269-2919.5US

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APPEAL BRIEF

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Attn: Board of Patent Appeals and Interferences

Sir:

This Appeal Brief is being submitted in the format required by 37 C.F.R. § 41.37(c)(1), with the fee required by 37 C.F.R. § 41.20(b)(2).

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I. REAL PARTY IN INTEREST

U.S. Application Serial No. 09/944,506 (hereinafter "the '506 Application"), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc., as evidenced by the assignment that has been recorded with the U.S. Patent & Trademark Office (hereinafter "the Office") at Reel No. 008618, Frame No. 0703. Accordingly, Micron Technology, Inc., is the real party in interest in the above-referenced appeal.

II. RELATED APPEALS AND INTERFERENCES

Neither Appellants nor the undersigned attorney are aware of any action pending before the Board of Patent Appeals and Interferences (hereinafter "the Board") that would affect or influence the Board's decision in the above-referenced appeal.

III. STATUS OF CLAIMS

The above-referenced application was filed with twenty-four (24) claims.

Claims 8 and 15-17 have been canceled without prejudice or disclaimer.

Accordingly, claims 1-7, 9-14, and 18-24 remain pending and under consideration in the above-referenced application.

Claims 1-6, 13, 14, and 18-24 are subject to final rejections, which are to be reviewed in the above-referenced appeal.

Claims 7 and 9-12 have been allowed.

IV. STATUS OF AMENDMENTS

The '506 Application was filed on September 16, 2003, with twenty-four (24) claims.

A first action on the merits of claim 1-24 was mailed on October 7, 2003. All of the claims were rejected in that Office Action. An Amendment was filed on January 12, 2004, in response to the first Office Action. The Amendment included formal revisions to the claims, as well as explanations as to the patentability of the claims over the numerous objections and rejections that had been presented in the first Office Action.

On April 22, 2004, a second, Final Office Action was mailed. While some of the prior grounds for rejecting the claims were withdrawn, the majority with maintained. Appellants responded by filing an Amendment Under 37 C.F.R. § 1.116 on June 25, 2004, in which the title of the above-referenced application was revised.

Evidently, the Examiner was somewhat convinced by the further reasoning as to the patentability of the claims provided in the Amendment Under 37 C.F.R. § 1.116. The finality of the April 22, 2004, Office Action was withdrawn, and a third, non-final action was issued on July 21, 2004. In the third Office Action, claims 7 and 9-12 were allowed, and claims 5, 14, 20, and 22 were apparently drawn to allowable subject matter. In addition, some of the prior grounds of rejection were maintained and a new ground of rejection was presented. In response to the third action, another Amendment was filed on October 25, 2004. Independent claims 1 and 18 were revised and claims 15-17 were canceled without prejudice or disclaimer. In addition, remarks were provided to show the allowability of the claims that were still rejected.

A fourth, Final Office Action followed on January 11, 2005. That Final Office Action indicated that claims 7 and 9-12 were allowable, but that claims 1-6, 8, 13, and 18-24 were not.

In an Amendment Under 37 C.F.R. § 1.116 dated March 11, 2005, Appellants made a final attempt to convince the Examiner that the rejected claims are indeed patentable. In addition, claim 8 was canceled, reducing the number of issues that remained for appeal.

The Examiner maintained his rejections in an Advisory Action dated March 29, 2005, and refused to cancel claim 8.

Accordingly, a Notice of Appeal was mailed to the Office on April 7, 2005, and is followed by this Appeal Brief, which is being filed within two months of the filing date of Notice of Appeal.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claims 1-6 of the '506 Application are directed to a precursor to a semiconductor device structure. That precursor includes a semiconductor device layered structure with at least one trench formed therein. A buffer film layer is located over at least a portion of a semiconductor substrate of the semiconductor device layered structure. At least one shallow trench isolation (STI) structure is positioned at least partially within the trench. The at least one STI structure includes a substantially flat surface and an integral ledge. The integral ledge extends laterally outward and contacts only an areas of an active surface of the semiconductor substrate that is located adjacent to the at least one trench. There is no discernable boundary between the integral ledge and a remainder of the at least one STI structure.

Claims 13 and 14 recite an intermediate semiconductor device structure that includes a semiconductor substrate with at least one trench formed therein and at least one trench isolation structure. The at least one trench isolation structure includes a portion that extends laterally over

and contacts only a portion of the active surface of the substrate located adjacent to a corner formed between the active surface and a wall of the trench. This configuration electrically isolates the at least one trench corner.

Claims 18-24 are drawn to a precursor to a semiconductor device structure. The precursor includes a semiconductor substrate and at least one trench formed in the semiconductor substrate. In addition, the precursor includes a buffer film layer over an active surface of the semiconductor substrate. At least one STI structure is located at least partially within the at least one trench, and is exposed through the buffer film layer. The at least one STI structure includes at least one integral ledge that extends laterally outward from the trench to contact an area of the active surface of the substrate located adjacent to the trench. There is no discernable boundary between the ledge and the remainder of the STI structure.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) Claim 8 stands rejected under 35 U.S.C. § 101 as reciting the same invention as that to which claims 5-12 of prior U.S. Patent 6,322,634 (hereinafter "the '634 Patent") are drawn;

(B) Claims 1-6 and 18-24 stand rejected under 35 U.S.C. § 112, first paragraph, for allegedly reciting subject matter that is not adequately described in the above-referenced application;

(C) Claim 13 stands rejected under 35 U.S.C. § 102(b) for reciting subject matter which is purportedly anticipated by that described in U.S. Patent 5,521,422 to Mandelman et al. (hereinafter "Mandelman"); and

(D) Claim 13 also stands rejected under 35 U.S.C. § 102(b) for being directed to subject matter which is allegedly anticipated by the subject matter described in U.S. Patent 5,506,168 to Morita et al. (hereinafter "Morita").

VIII. ARGUMENT

A. DOUBLE PATENTING REJECTION UNDER 35 U.S.C. § 101

Claim 8 stands rejected under 35 U.S.C. § 101 as reciting the same invention as that to which claims 5-12 of the '634 Patent are drawn.

1. LEGAL AUTHORITY

35 U.S.C. § 101 provides in relevant part: "Whoever invents or discovers any new and useful process . . . may obtain *a* patent therefor . . . " (emphasis added). In explaining the basis on which a double patenting rejection under 35 U.S.C. § 101 should be premised, M.P.E.P. § 804(II)(A) provides:

> In determining whether a statutory basis for a double patenting rejection exists, the question to be asked is: Is the same invention being claimed twice?
>
> . . . Is there an embodiment of the invention that falls within the scope of one claim, but not the other? If there is such an embodiment, then identical subject matter is not defined by both claims and statutory double patenting would not exist.

2. ANALYSIS

Claim 8, even when read together with independent claim 7, does not include all of the limitations of any of claims 5-12 of the '634 Patent.

Independent claim 5 of the '634 Patent, as well as claims 6, 7, and 12 depending therefrom, are directed to intermediate semiconductor device structures with buffer film layers that must comprise substantially oxidation resistant materials. There is no such requirement in claim 8 of the above-referenced application. Therefore, claim 8 of the above-referenced application differs in scope from claims 5-7 and 12 of the '634 Patent and, thus, should not be subject to a statutory double patenting rejection.

None of the intermediate semiconductor device structures of claims 8-10 of the '634 Patent includes a buffer film layer, as is required by claim 8 of the above-referenced application. Accordingly, claim 8 of the above-referenced application differs in scope from claims 8-10 of the '634 Patent and, therefore, should not be subject to a statutory double patenting rejection.

Claim 11 of the '634 Patent depends from claim 1, which has been omitted from the Examiner's grounds for rejecting claim 8 under 35 U.S.C. § 101. In any event, claim 11 and claim 1 include a number of method limitations that do not appear in claim 8 of the above-referenced application. Therefore, claim 8 of the above-referenced application is not identical in scope to claim 11 of the '634 Patent and should not be subject to a statutory double patenting rejection.

In view of the foregoing, it is clear that the 35 U.S.C. § 101 double patenting rejection of claim 8 should be reversed and that claim 8 should be allowed.

B. REJECTIONS UNDER 35 U.S.C. § 112, FIRST PARAGRAPH

Claims 1-6 and 18-24 stand rejected under 35 U.S.C. § 112, first paragraph, for allegedly reciting subject matter that is not adequately described in the above-referenced application

1. LEGAL AUTHORITY

The exact language recited in the claims need not be found verbatim in the originally-filed specification to be supported by the originally-filed specification. M.P.E.P. § 2173.05(f) (which applies to 35 U.S.C. § 112, second paragraph, indefiniteness rejections, provides "[t]here is no requirement that the words in the claim must match those used in the specification disclosure.").

2. ANALYSIS

The Examiner has objected to the recitation "with no discernable boundary between the integral edge and a remainder of the at least one shallow trench isolation structure." Final Office Action, page 2.

Contrary to the Examiner's assertion in the remarks that accompanied the Advisory Action, the mere fact that different reference characters are used to identify the STI structure 126 and features thereof, such as integral ledges 130, does not mean that there must be a discernable boundary between these features.

It is respectfully submitted that the specification and drawings of the above-referenced application provide an adequate written description for a structure in which there is no discernable boundary between at least one STI structure and its integral ledge. Specifically,

Figs. 7-10 and paragraphs **[0020]** and **[0021]** of the above-referenced application describe an example of a process by which an STI structure and its integral ledge are formed from a single layer of isolation material 122. The isolation material 122 is deposited over a semiconductor substrate 102 and within at least one shallow trench 112 formed in the semiconductor substrate 102. Fig. 7; paragraph **[0020]**. The isolation material 122 is then removed down to a buffer film layer 106 that overlies the semiconductor substrate 102, forming an STI structure 126 that includes integral ledges 130. Fig. 8; paragraph **[0021]**.

As the *entire* STI structure 126, including its integral ledges 130, are formed from the same layer of isolation material 122, there could not be a discernable boundary between the ledges 130 and the remainder of the STI structure 126.

As such, it is apparent that the specification of the above-referenced application provides an adequate written description of an example of an STI structure "with no discernable boundary" between a ledge and the remainder thereof. Therefore, independent claims 1 and 18 comply with the written description requirement of the first paragraph of 35 U.S.C. § 112. Accordingly, withdrawal of the 35 U.S.C. § 112, first paragraph rejections of independent claims 1 and 18, as well as the rejections of claims 2-6 and 19-24 depending respectively therefrom, is respectfully requested.

C. REJECTIONS UNDER 35 U.S.C. § 102

Claim 13 stands rejected under 35 U.S.C. § 102(b).

1. LEGAL AUTHORITY

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

2. REFERENCES RELIED UPON

Mandelman

Mandelman describes (at col. 5, lines 3-23) and illustrates (in FIG. 4c) a precursor to a semiconductor device structure that includes a semiconductor substrate 10 with trenches 16 formed therein. The trenches 16 of the semiconductor substrate 10 are lined with a thermal oxide 34, as are areas of the active surface of the semiconductor substrate 10 that are located adjacent to the trenches 16. STI structures 18 fill the remaining space within the trenches, and include corner dielectrics 22c that extend laterally over regions of the active surface of the semiconductor substrate 10 that are located adjacent to the trenches 16. The thermal oxide 34 prevents the STI structures 18a and their corner dielectrics 22c from contacting any portion of the semiconductor substrate 10; the STI structures 18a and their corner dielectrics 22c instead contact the thermal oxide 34 that lines the trenches 16 and regions of the active surface of the semiconductor substrate 10 that are adjacent to the trenches 16.\

Morita

Morita discloses several embodiments of STI structures, most of which include a central region 3 that fills a trench 2, as well as a separately formed spacer 5 that extends laterally over regions of the active surface of a semiconductor substrate 1 that are located adjacent to the trench 2. *See, e.g.,* FIGS. 6, 7, and 9. As these spacers 5 are fabricated separately from the central regions 3 of the STIs, a discernable boundary will be present between the spacers 5 and the central regions 3. In the STI embodiments that are depicted in FIGS. 6, 7, and 10 of Morita, a silicon oxide film 11 separates the spacers 5 from the active surface of the semiconductor substrate 1.

The only embodiment of an STI that includes an integral laterally extending ledge is shown in FIG. 72. More specifically, FIG. 72 of Morita shows an intermediate semiconductor device structure that includes a semiconductor substrate 1 with at least one trench 2 formed therein, silicon oxide films 11 and 36 lining the active surface of the semiconductor substrate 1 and the surfaces of the trench 2, respectively, and a silicon nitrogen film 37 filling the at least one trench. *See also,* col. 13, lines 19-26. As FIG. 72 clearly depicts, the surface of the silicon nitrogen film 37 tapers at the edges thereof.

3. ANALYSIS

a. MANDELMAN

Claim 13 stands rejected under 35 U.S.C. § 102(b) for reciting subject matter which is purportedly anticipated by that described in U.S. Patent 5,521,422 to Mandelman et al. (hereinafter "Mandelman").

Independent claim 13 is drawn to an intermediate semiconductor device structure that includes a semiconductor substrate with at least one trench formed therein, and a trench isolation structure within the at least one trench. The trench isolation structure also extends laterally over and contacts a portion of the active surface of the semiconductor substrate adjacent to a trench corner.

As Mandelman does not expressly or inherently describe an intermediate semiconductor device structure that includes a trench isolation structure that extends laterally over and contacts a portion of the active surface of a semiconductor substrate adjacent to a trench corner, Mandelman does not anticipate each and every element of independent claim 13. It is, therefore, respectfully submitted that independent claim 13 is drawn to subject matter that, under 35 U.S.C. § 102(b), is allowable over the subject matter disclosed in Mandelman.

b. MORITA

Claim 13 is also rejected under 35 U.S.C. § 102(b) for being directed to subject matter which is allegedly anticipated by the subject matter described in U.S. Patent 5,506,168 to Morita et al. (hereinafter "Morita").

In addition to requiring that the ledges of an STI structure contact an active surface of a semiconductor substrate, independent claim 13 also requires that the at least one shallow trench isolation structure have a substantially flat surface.

The only embodiment of an STI that includes an integral laterally extending ledge is shown in FIG. 72. More specifically, FIG. 72 of Morita shows an intermediate semiconductor device structure that includes a semiconductor substrate 1 with at least one trench 2 formed

therein, silicon oxide films 11 and 36 lining the active surface of the semiconductor substrate 1 and the surfaces of the trench 2, respectively, and a silicon nitrogen film 37 filling the at least one trench. *See also,* col. 13, lines 19-26. As FIG. 72 clearly depicts, the surface of the silicon nitrogen film 37 tapers at the edges thereof.

As none of the STI structures disclosed in Morita contacts an active surface of a semiconductor substrate or has a substantially flat surface, Morita does not anticipate each and every element of independent claim 13. As such, it is respectfully submitted that, under 35 U.S.C. § 102(b), the subject matter to which independent claim 13 is drawn is allowable over the subject matter described in Morita.

In view of the foregoing, reversal of the 35 U.S.C. § 102(b) rejections of claim 13 is respectfully solicited.

VIII. CLAIMS APPENDIX

The current status of each claim that has been introduced into the above-referenced application is set forth in CLAIMS APPENDIX to this Appeal Brief.

IX. EVIDENCE APPENDIX

There is no EVIDENCE APPENDIX to this Appeal Brief.

X. RELATED PROCEEDINGS APPENDIX

No decisions have been rendered by the Board or any court in a related application. Therefore, this Appeal Brief is not accompanied by a RELATED PROCEEDINGS APPENDIX.

XI. CONCLUSION

It is respectfully submitted that:

(A) Claim 8 is allowable under 35 U.S.C. § 101 for reciting subject matter that differs in scope from the subject matter recited in claims 5-12 of the '634 Patent;

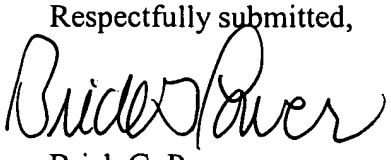
(B) Claims 1-6 and 18-24 are allowable under 35 U.S.C. § 112, first paragraph, for reciting subject matter that is adequately described in the specification and drawings of the above-referenced application;

(C) Claim 13 is allowable under 35 U.S.C. § 102(b) for reciting subject matter which is patentable over that described in Mandelman; and

(D) Claim 13 is also allowable under 35 U.S.C. § 102(b) for being directed to subject matter that is novel over the subject matter described in Morita.

Accordingly, it is respectfully requested that the rejections of claims 1-6, 13, 14, and 18-24 be reversed and that each of these claims be allowed.

Respectfully submitted,



Brick G. Power
Registration No. 38,581
Attorney for Applicant
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: June 7, 2005
BGP/eg
Document in ProLaw

CLAIMS APPENDIX

1. (Previously presented) A precursor to a semiconductor device structure, comprising:

a semiconductor device layered structure comprising a semiconductor substrate;

a buffer film layer located over at least a portion of the semiconductor substrate;

at least one trench formed in the semiconductor device layered structure; and

at least one shallow trench isolation structure positioned at least partially within the at least one trench and including:

a substantially flat surface; and

an integral ledge which extends laterally outward from the at least one trench, with no discernable boundary between the integral ledge and a remainder of the at least one shallow trench isolation structure, so as to contact only an area of an active surface of the semiconductor substrate adjacent the at least one trench.

2. (Previously presented) The precursor of claim 1, wherein the buffer film layer comprises substantially oxidation resistant material.

3. (Previously presented) The precursor of claim 2, wherein the substantially oxidation resistant material is selectively etchable.

4. (Previously presented) The precursor of claim 1, wherein a lateral edge of the integral ledge contacts the buffer film layer.

5. (Previously presented) The precursor of claim 1, wherein the at least one shallow trench isolation structure comprises densified material.

6. (Previously presented) The precursor of claim 1, wherein the buffer film layer comprises silicon nitride.

7. (Previously presented) An intermediate semiconductor device structure, comprising:

a semiconductor substrate including at least one trench formed therein and at least one trench corner located at a juncture between the at least one trench and an active surface of the semiconductor substrate; and

a buffer film layer over at least portions of the active surface; and

at least one densified trench isolation structure including a substantially flat surface exposed through the buffer film layer, the at least one trench corner being covered by the at least one densified trench isolation structure.

8. (Previously presented) The intermediate semiconductor device structure of claim 7, wherein the buffer film layer comprises a substantially oxidation resistant material

9. (Previously presented) The intermediate semiconductor device structure of claim 7, further comprising:

a layer comprising silicon oxide disposed within the at least one trench and between the semiconductor substrate and the buffer film layer.

10. (Previously presented) The intermediate semiconductor device structure of claim 9, wherein the layer comprises densified silicon dioxide.

11. (Previously presented) The intermediate semiconductor device structure of claim 7, wherein the at least one densified trench isolation structure comprises densified material.

12. (Previously presented) The intermediate semiconductor device structure of claim 7, wherein the buffer film layer comprises silicon nitride.

13. (Previously presented) An intermediate semiconductor device structure, comprising:

a semiconductor substrate including at least one trench formed therein and at least one trench corner located at a juncture between the at least one trench and an active surface of the semiconductor substrate; and

at least one trench isolation structure including a substantially flat surface, the at least one trench isolation structure extending laterally over and contacting only a portion of the active surface adjacent the at least one trench corner so as to electrically isolate the at least one trench corner.

14. (Previously presented) The intermediate semiconductor device structure of claim 13, wherein the at least one trench isolation structure comprises densified silicon dioxide.

15-17. (Canceled)

18. (Previously presented) A precursor to a semiconductor device structure, comprising:

a semiconductor substrate;

at least one trench formed in the semiconductor substrate;

a buffer film layer over an active surface of the semiconductor substrate;

and at least one shallow trench isolation structure at least partially within the at least one trench and exposed through the buffer film layer, the at least one shallow trench isolation structure including at least one integral ledge extending laterally outward from the at least one trench, with no discernable boundary between the at least one integral ledge and a remainder of the at least one shallow trench isolation structure, so as to contact an area of the active surface adjacent the at least one trench.

19. (Previously presented) The precursor of claim 18, wherein the at least one shallow trench isolation structure includes a substantially planar surface.

20. (Previously presented) The precursor of claim 18, wherein the at least one shallow trench isolation structure comprises densified silicon oxide.

21. (Previously presented) The precursor of claim 18, wherein the buffer film layer comprises silicon nitride.

22. (Previously presented) The precursor of claim 18, wherein the buffer film layer comprises densified material.

23. (Previously presented) The precursor of claim 18, wherein the buffer film layer comprises substantially oxidation resistant material.

24. (Previously presented) The precursor of claim 23, wherein the substantially oxidation resistant material is selectively etchable.

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(to be used for all correspondence after initial filing)

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First Named Inventor	Pai-Hung Pan
Group Art Unit	2823
Examiner Name	G. Fourson III
Attorney Docket Number	2269-2919.5US (96-0499.02/US)

ENCLOSURES *(check all that apply)*

- [x] Postcard receipt acknowledgment (attached to the front of this transmittal)
- [x] Duplicate copy of this transmittal sheet in the event that additional filing fees are required under 37 C.F.R. § 1.16
- [ ] Preliminary Amendment
- [ ] Response to Restriction Requirement/Election of Species Requirement dated
- [ ] Amendment in response to office action dated
- [ ] Amendment under 37 C.F.R. § 1.116 in response to final office action dated
- [ ] Additional claims fee - Check No. in the amount of $
- [ ] Letter to Chief Draftsman and copy of FIGS. with changes made in red
- [ ] Transmittal of Formal Drawings
- [ ] Formal Drawings (sheets)
- [ ] Information Disclosure Statement, PTO/SB/08A (08-00); [ ] copy of cited references
- [ ] Supplemental Information Disclosure Statement; PTO/SB/08A (08-00); copy of cited references and Check No. in the amount of $180.00
- [ ] Associate Power of Attorney
- [ ] Petition for Extension of Time and Check No. in the amount of $
- [ ] Petition
- [x] Appeal Brief (15 pages) Claims Appendix (5 pages) and Check No. 7913 in the amount of $500.00
- [ ] Certified Copy of Priority Document(s)
- [ ] Assignment Papers *(for an Application)*
- [ ] Terminal Disclaimer
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- [ ] Terminal Disclaimer
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Remarks

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	Brick G. Power — Registration No. 38,581
Signature	Brick Power
Date	June 7, 2005

CERTIFICATE OF MAILING

Express Mail Label Number: EL994843912US

Date of Deposit: June 7, 2005

Person Making Deposit: Steve Wong